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#6

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet

1

of

1

Complete if Known

Application Number	Not assigned
Filing Date	June 28, 2001
First Named Inventor	SOLOMON et al
Group Art Unit	Not assigned
Examiner Name	Not assigned
Attorney Docket Number	2207/10607

09/892566
16/28/01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
GJP		5,381,533		PELEG et al	Jan. 10, 1995	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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GJP		Jourdan et al, "eXtended Block Cache", Proceedings of Int'l. Symposium on High Performance Computer Architecture, pp 1-10, January 2000	

Examiner Signature

GARY J. PORTKA

Date Considered

10/27/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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sheet 1 of 1

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GJP		Bellas et al, "Architectural and Compiler Techniques for Energy Reduction in High Performance Microprocessors", <i>IEEE Transactions on VLSI</i> , Vol. 8, No. 3, June 2000	
↑		Black et al, "The Block-Based Trace Cache", Proceedings of the 26th Intl. Symposium on Computer Architecture, IEEE Computer Society TCCA, ACM SIGARCH, Atlanta, Georgia, May 2-4, 1999	
		Friendly et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", 30th Annual IEEE/ACM Intl. Symposium on Microarchitecture, Research Triangle Park, North Carolina, December 1-3, 1997	
		Intrater et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", 19th Annual Intl. Symposium on Computer Architecture, Gold Coast, Australia, May 19-21, 1992	
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		Glaskowsky, Peter N., "Pentium 4 (Partially) Previewed", <i>Microprocessor Report</i> , Vol. 14, Archive 8, pp. 1, 11-13, August 2000	
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↓		Upton, Michael, "The Intel Pentium® 4 Processor", http://www.intel.com/pentium4 , October 2000	
GJP		Rotenberg et al, "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings, 29th Annual IEEE/ACM Intl. Symposium on Microarchitecture, MICRO-29, IEEE Computer Society Tech. Comm. on Microprogramming and Microarchitecture, Assn. for Computing Machinery SIGMICRO, Paris, France, December 2-4, 1996	
Examiner Signature	GARY J. PORTKA		Date Considered 10/27/03

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